UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,658	12/12/2001	Scott Demer	400.105US01	7933

27073 7590 05/21/2003

LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
NGUYEN, TAN	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/017,658	Applicant(s) DERNER ET AL.
	Examiner Tan T. Nguyen	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8-17,21 and 22* is/are pending in the application.

4a) Of the above claim(s) *5-7 and 18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-17,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. The following action is in response to the Amendment and Response filed by Applicants on April 15, 2003.

2. Claims 1-4, 8-17 and 21-22 are pending.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 9-12, 14-16, 17, 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Takasugi (U.S. Patent No. 5,663,906).

Regarding claims 1, 14 and 17, Takasugi discloses in figures 1-2 a semiconductor memory device comprises a memory array [10] (column 3, line 57). The memory cell array [10] is made up of a plurality of subarrays [10_1-10_n]. Further, the memory cell array [10] comprises a DROM (DRAM and ROM) unit [10A] comprised of memory cells which serve as volatile memory (DRAM) (column 9, lines 58-59, 63 to column 10, line 5), and memory cells serve as a non-volatile memory (ROM) (column 3, line 66 to column 4, line 5). Takasugi further discloses each of the subarrays [10_1-10_n] includes a pair of complementary bit lines [BL_i,/BL_i] (column 4, line 7) coupled to the memory cells and a sense amplifier [12_i] (column 4, line 29). A first conductive line [13_i] having the same potential as the power supply potential (Vcc level) and a second conductive line [/13_i] having the same potential as the ground potential (Vss level) are disposed in the DROM unit [10A] of the subarray [10] (column 4, lines 52-56). Takasugi discloses one transistor/one capacitor type memory cells [$11_{k,l}$] are respectively

electrically connected to points where the bit line pairs and the word lines intersect respectively (column 4, lines 12-16). The memory cell [$11_{k,l}$] is made up of a capacitor [$C_{k,l}$] and an n-channel transistor [$T_{k,l}$] for the charge transfer (column 4, lines 16-18).

Takasugi teaches that the memory cells which stored fixed data "1" (HIGH LEVEL) therein of the memory cells serving as the ROM of the DROM unit [10A] i.e. memory cells [$11_{1,l}$, $11_{2,l}$, $11_{5,l}$, $11_{6,l}$] are electrically connected to either the first conductive line [13_i] or the second conductive line [$/13_i$] (column 4, lines 56-61). As Takasugi disclosed the memory cells coupled to the first conductive line [13_i] so that the memory cells store data "1", it inherently teaches the memory cells are hard programmed to a first data state.

Regarding claim 9, Takasugi disclosed in figure 6 a second embodiment has a DROM unit [10A] and a DRAM unit [10B] provided in a manner similar to the memory device in Figure 1. In the second embodiment only a conductive line [13_i] is provided (column 11, line 34-39) to render memory cells [$11_{1,l}$, $11_{5,l}$] ROM cells. The other memory cells [$11_{2,l}$, $11_{4,l}$, $11_{6,l}$] of the DROM unit [10A] do not have the conductive line, are DRAM cells as disclosed in column 4, lines 1-6).

Regarding claims 2 and 10, Takasugi disclosed the cells [$11_{1,l}$, $11_{2,l}$, $11_{5,l}$, $11_{6,l}$] are ROM cells having transistors [$T_{1,l}$, $T_{2,l}$, $T_{5,l}$, $T_{6,l}$] coupled to either the bit line [BL_i] or [$/BL_i$], and the cells [$11_{m-2,l}$, $11_{m,l}$] are the DRAM cells having transistors [$T_{m-2,l}$, $T_{m,l}$] coupled to either the bit line [BL_i] or [$/BL_i$]. The gate of the ROM cells [$11_{1,l}$, $11_{2,l}$, $11_{5,l}$, $11_{6,l}$] and the gate of the DRAM cells [$11_{m-2,l}$, $11_{m,i}$] are coupled to different word lines [WL_1-WL_6] and [WL_{m-2}, $WL_{m,l}$].

Regarding claims 3-4, 11-12, 15-16, 21-22, Takasugi disclosed that the ROM cells are coupled to either the first conductive line [13_i] which has potential [Vcc] or the second conductive line [$/13_i$] which has potential [V_{ss}] (column 4, lines 56-61).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takasugi in view of Koga (U.S. Patent No. 5,675,547).

7. See description of Takasugi in paragraph 4, supra. Takasugi does not disclose the capacitor of the ROM cell is hard programmed by shoring the dielectric layer of the capacitor.

8. Koga discloses a volatile storage device including a non-volatile storage block. Koga further discloses the semiconductor storage device comprises a plurality of first memory cells for storing volatile information. A plurality of second memory cells for nonvolatily storing information. Each of the second memory cells having a cell selecting transistor and a capacitor connected at one end of the selecting transistor. A nonvolatile information storage control means for selectively applying a given voltage to the other end of the capacitor to thereby destroy the capacitor and nonvolatily store information into the second memory cells.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory device of Takasugi by providing the nonvolatile storage control means of Koga.

The rationale is as follows: A person of ordinary skill in the art at the time the invention was made would have been motivated to use the non-volatile storage control means of Koga to destroy the dielectric film constituting the capacitor to convert the volatile cell to a non-volatile cell.

9. Applicant's arguments with respect to claims 1-4, 8, 14-17 and 21-22 have been considered but are moot in view of the new ground(s) of rejection.

10. REMARKS

Applicants asserted in the Remarks that Takasugi does not teach the hard programming of a memory cell. In view of Applicant's assertion, Takasugi discloses the memory cells in the DROM unit [10B] are coupled to either the first conductive line [13_i], which has a potential [Vcc], or the second conductive line [$/13_i$], which has potential [Vss] to render the memory cells storing fixed data "1" (column 4, lines 56-60). The connection of the conductive line to the memory cells to render the cells storing fixed data would be considered as hard programming the memory cells.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (703) 308-1298. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Tan T. Nguyen
Primary Examiner
Art Unit 2818
May 16, 2003